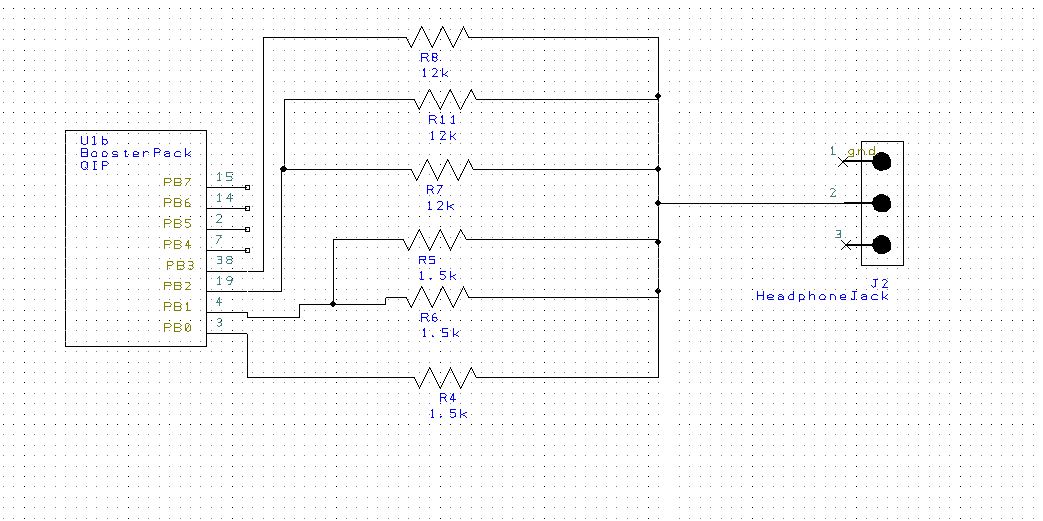
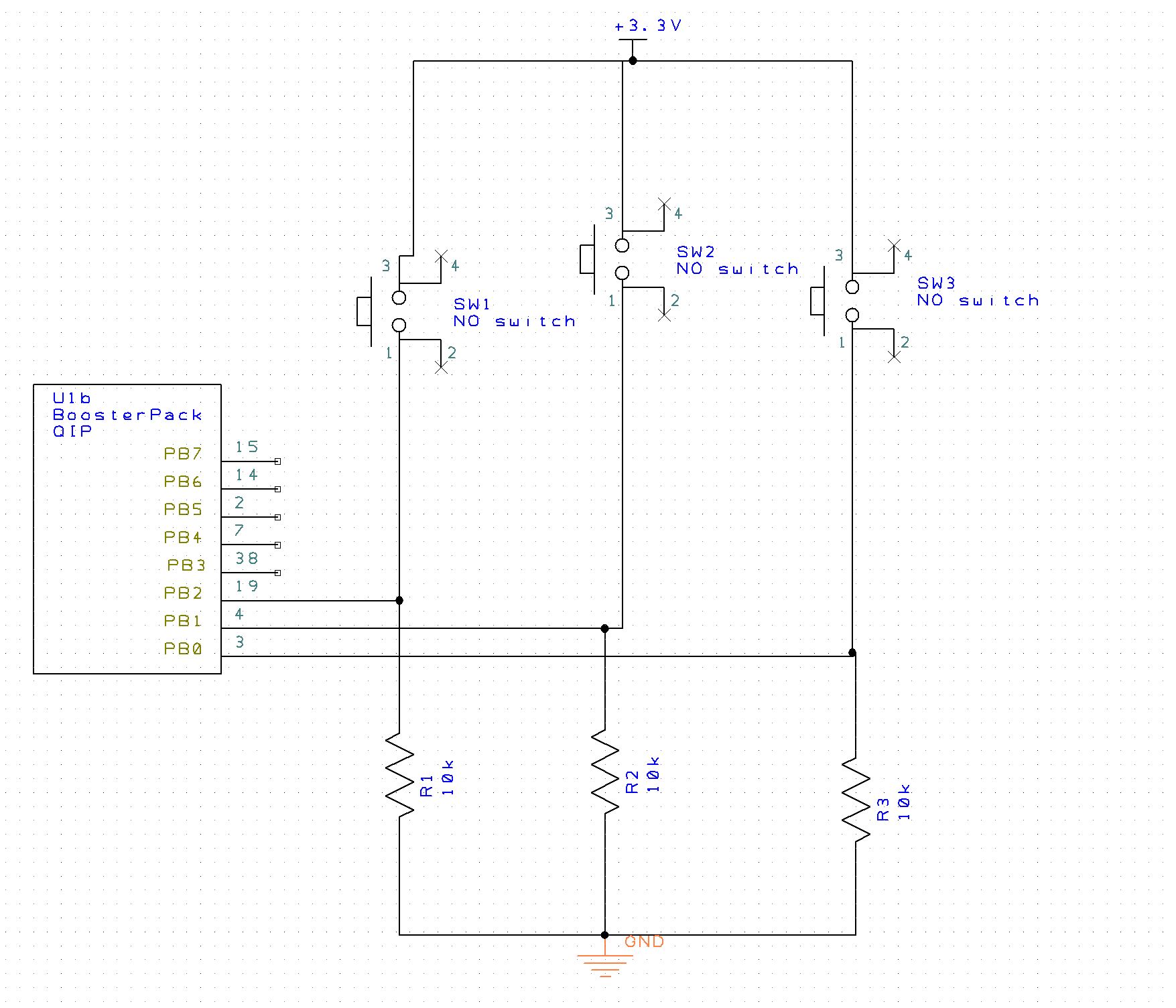
**Lab 6 Deliverables**

Akaash Chikarmane and Milan Feliciello

Section: 16085

Spring 2016

**Schematic**

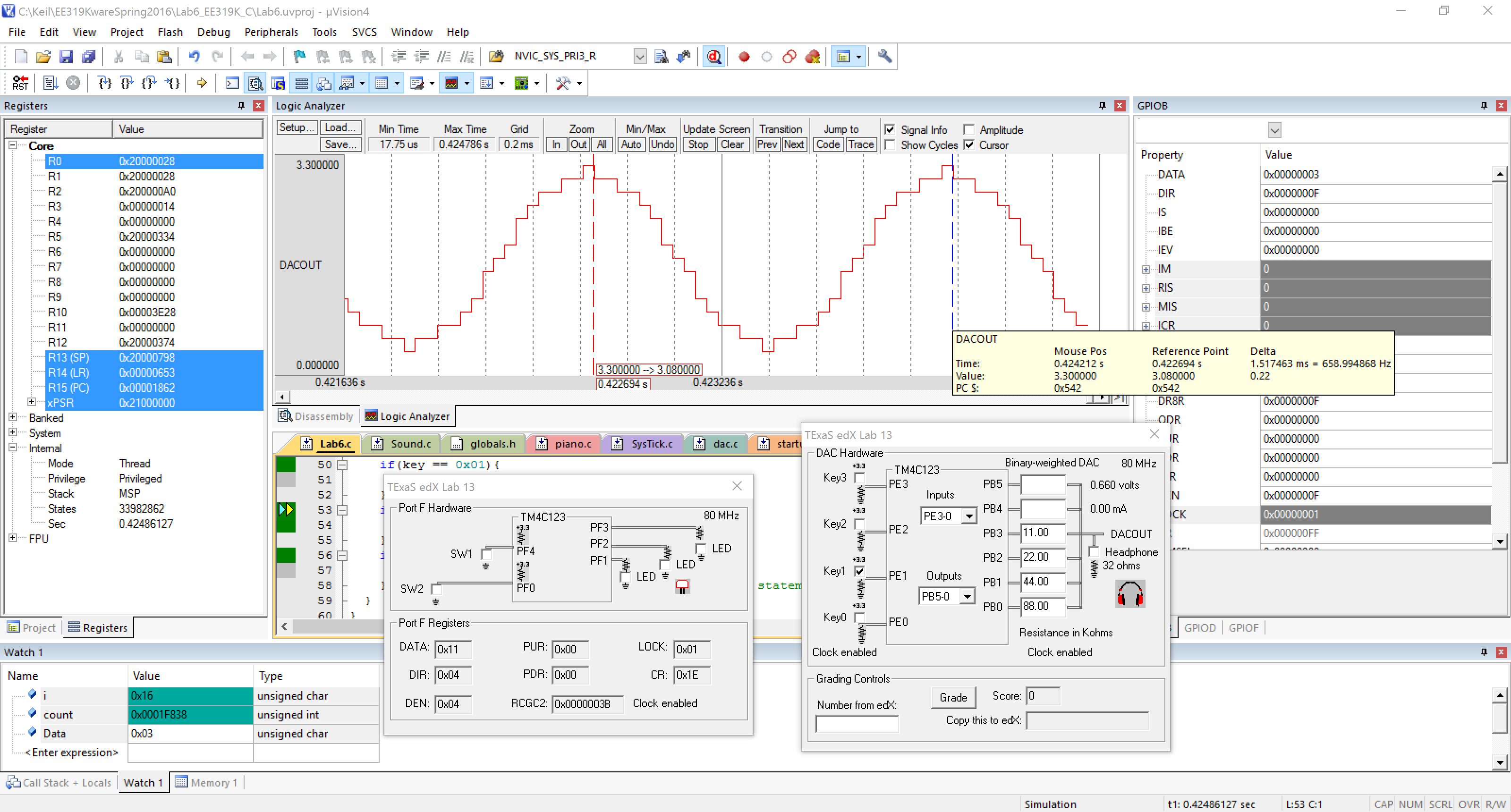


**Software Design**

1. **Data Structure**

|  |  |
| --- | --- |
| 0 | 8 |
| 1 | 9 |
| 2 | 11 |
| 3 | 12 |
| 4 | 13 |
| 5 | 13 |
| 6 | 14 |
| 7 | 14 |
| 8 | 15 |
| 9 | 14 |
| 10 | 14 |
| 11 | 13 |
| 12 | 13 |
| 13 | 12 |
| 14 | 11 |
| 15 | 9 |
| 16 | 8 |
| 17 | 7 |
| 18 | 5 |
| 19 | 4 |
| 20 | 3 |
| 21 | 3 |
| 22 | 2 |
| 23 | 2 |
| 24 | 1 |
| 25 | 2 |
| 26 | 2 |
| 27 | 3 |
| 28 | 3 |
| 29 | 4 |
| 30 | 5 |
| 31 | 7 |

**Dual Scope (Logic Analyzer)**

****

**Measurement Data**

|  |  |  |
| --- | --- | --- |
| **Bit 3 bit 2 bit 1 bit 0** | **Theoretical DAC Voltage** | **Measured DAC Voltage** |
| **0** | 0 | 0.6 mV |
| **1** | .22 | 0.214 |
| **2** | .44 | 0.451 |
| **3** | .66 | 0.665 |
| **4** | .88 | 0.881 |
| **5** | 1.1 | 1.095 |
| **6** | 1.32 | 1.332 |
| **7** | 1.54 | 1.546 |
| **8** | 1.76 | 1.759 |
| **9** | 1.98 | 1.973 |
| **10** | 2.2 | 2.21 |
| **11** | 2.42 | 2.424 |
| **12** | 2.64 | 2.64 |
| **13** | 2.86 | 2.854 |
| **14** | 3.08 | 3.091 |
| **15** | 3.3 | 3.304 |

Resolution: 3.3/(16-1) = .22

Range: 3.3 V

Precision: 16 levels

Accuracy: (3.3-3.304)/(3.3) = -0.00121212121

**Questions**

a. The interrupt trigger occurs every time the NVIC\_ST\_CURRENT\_R reaches 0 and sets the interrupt flag.

b. The interrupt vector is declared in Startup.s.

c. When the interrupt flag is detected the address of the interrupt vector is put into the PC and the address of the next instruction to return to. Then the interrupt vector is executed.

d. The link register contains the address of the next instruction to be executed, that is put into the PC and execution of the main program continues.